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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,303	03/24/2004	Yukihiro Ushiku	04329.2459-01	3815

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

EXAMINER	
MENZ, DOUGLAS M	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,303	USHIKU, YUKIHIRO	
	Examiner	Art Unit	
	Douglas M Menz	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi (US 5909626).

Regarding claim 9, Kobayashi discloses a semiconductor device comprising:

A semiconductor substrate (4) having a first region and a second region (Fig. 4E);

A buried insulating film (3) formed in the first region of the semiconductor substrate (Fig. 4E);

At least one first single crystalline semiconductor layer (9) having a semiconductor element formed therein and formed on the buried insulating film;

At least one second single crystalline semiconductor layer formed in the second region and in contact with the semiconductor substrate (*Vertical-type power element forming region*, Fig. 4E); and

An element isolation region (20) for isolating the single crystalline semiconductor layers from each other,

Wherein all the element isolation insulating films in the element isolation region (20) have the same height from the semiconductor substrate (Fig. 4E and Col. 7).

Regarding claim 10, Kobayashi further discloses wherein the first single crystalline semiconductor layer formed in the first region consists of a plurality of semiconductor layers (9,13) having a plurality of film thicknessess (Fig. 4E and Col. 7).

Regarding claims 11-12, Kobayashi further discloses wherein a CMOS element is formed in the first region and a bipolar element is formed in the second region (*vertical-type power element forming region*, Fig. 4E).

Regarding claims 13-16, Kobayashi further discloses wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor of the second region (*vertical-type power element forming region*, Fig. 4E); the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate (4, Fig. 4E); and the thickness of the semiconductor layer lower than a gate electrode of the MOS transistor is substantially the same thickness of the predetermined second single crystalline semiconductor layer (Fig. 4E).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following US patents disclose relevant semiconductor structures pertaining to bipolar and CMOS combinations: 5100810, 6235567, 6365447 and 6555891.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/16/04

DM

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800